## AMENDMENTS TO THE CLAIMS

1. (original) A heat sink attachment structure, comprising:

an integrated circuit chip mounted on a substrate surface;

a thermal interface layer in contact with said integrated circuit chip;

a heat sink in contact with said thermal interface layer; and

at least one spacer member in contact between said substrate surface and said heat sink, wherein said at least one spacer member is provided with an adhesive material on top and bottom surfaces thereof.

2. (currently amended) The structure of claim 1, wherein said at least one spacer member comprises a rigid material of a generally cylindrical shape.

3. (original) The structure of claim 2, wherein said at least one spacer member comprises phenolic.

4. (original) The structure of claim 1, wherein said thermal interface layer is adhesive free.

5. (original) The structure of claim 1, wherein said adhesive material provided on said at least one spacer member comprises a reworkable epoxy curable at room temperature.

6. (original) The structure of claim 1, wherein said thermal interface layer further comprises a thermal interface pad.

7. (original) The structure of claim 6, wherein said thermal interface pad has an initial thickness of about 6 mil and a compressed thickness of about 4 mils.



PAGE 4/8 * RCVD AT 7/7/2005 3:54:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/8 * DNIS:8729306 * CSID:8602860115 * DURATION (mm-ss):02-18

8. (original) A method for implementing attachment of a heat sink to and integrated circuit chip, the method comprising:

applying a thermal interface layer to the chip;

adhesively applying a first side of at least one spacer member to a substrate to which the chip is mounted;

aligning the heat sink to the chip; and

applying a load to the heat sink until the heat sink is adhesively bonded to a second side of said at least one spacer member.

9. (currently amended) The method of claim 8, wherein said at least one spacer member comprises a rigid material of a generally cylindrical shape.

10. (original) The method of claim 9, wherein said at least one spacer member comprises phenolic.

11. (original) The method of claim 8, wherein said thermal interface layer is adhesive free.

12. (original) The method of claim 8, wherein said adhesive material provided on said at least one spacer member comprises a reworkable epoxy curable at room temperature..

13. (original) The method of claim 8, wherein said thermal interface layer further comprises a thermal interface pad having an initial thickness of about 6 mil and a compressed thickness of about 4 mils.

14. (original) A semiconductor device packaging assembly, comprising:

a chip module mounted on a circuit board substrate;

at least one integrated circuit chip mounted on said chip module;



PAGE 5/8 * RCVD AT 7/7/2005 3:54:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/8 * DNIS:8729306 * CSID:8602860115 * DURATION (mm-ss):02-18

a thermal interface layer in contact with said at least one integrated circuit chip;

a heat sink in contact with said thermal interface layer; and

at least one spacer member in contact between said chip module and said heat sink, wherein said at least one spacer member is provided with an adhesive material on top and bottom surfaces thereof.

15. (currently amended) The semiconductor device packaging assembly of claim 14, wherein said at least one spacer member comprises a rigid material of a generally cylindrical shape.

16. (original) The semiconductor device packaging assembly of claim 15, wherein said at least one spacer member comprises phenolic.

17. (original) The semiconductor device packaging assembly of claim 14, wherein said thermal interface layer is adhesive free.

18. (original) The semiconductor device packaging assembly of claim 14, wherein said adhesive material provided on said at least one spacer member comprises a reworkable epoxy curable at room temperature.

19. (original) The semiconductor device packaging assembly of claim 14, wherein said thermal interface layer further comprises a thermal interface pad.

20. (original) The semiconductor device packaging assembly of claim 19, wherein said thermal interface pad has an initial thickness of about 6 mil and a compressed thickness of about 4 mils.



PAGE 6/8 * RCVD AT 7/7/2005 3:54:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/8 * DNIS:8729306 * CSID:8602860115 * DURATION (mm-ss):02-18